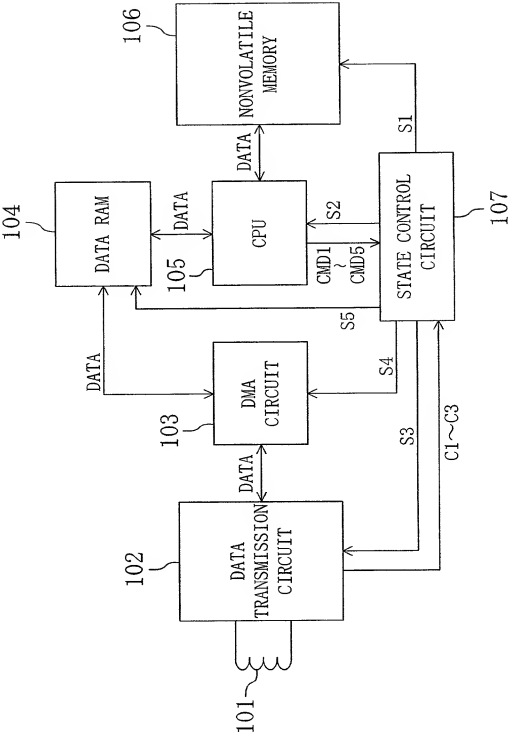
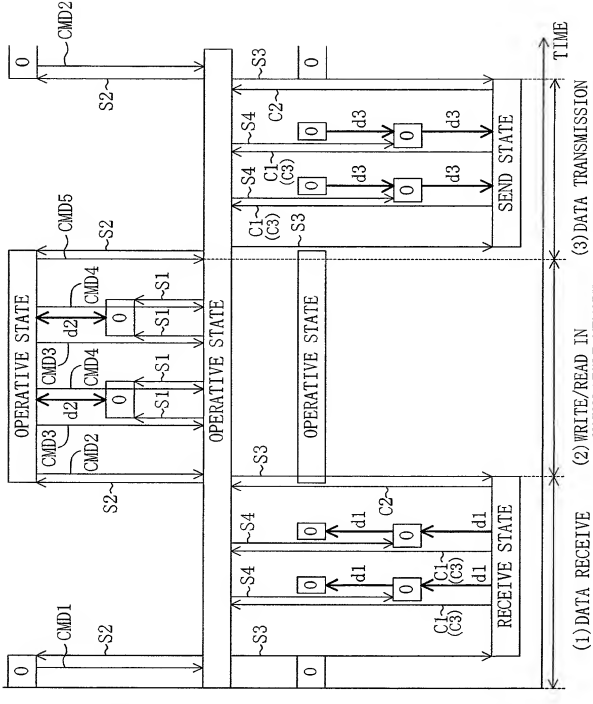
20060TO"2520E007

FIG. 1



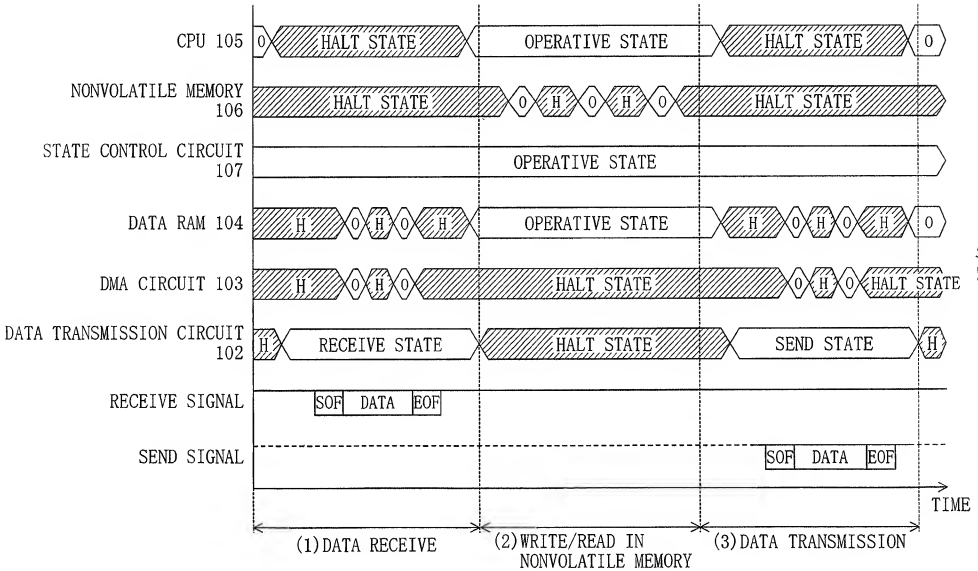
20010"4520501

FIG. 2



2060T0*2520E00T

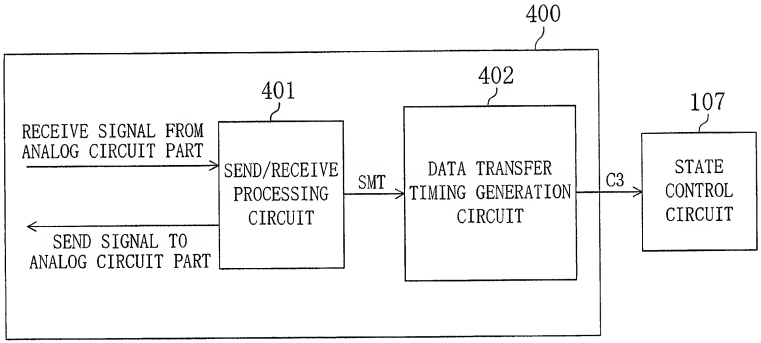
FIG. 3



10/030252

2060TO'2520E00T

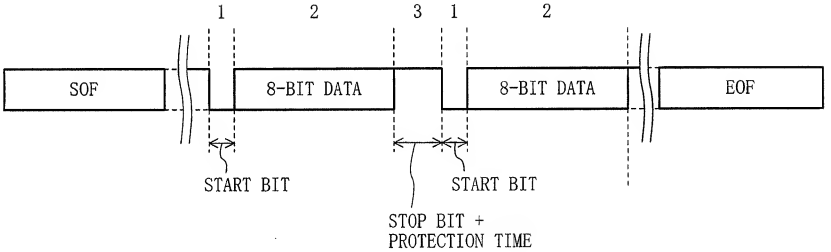
FIG. 4



10/030252

20607D*2520E001

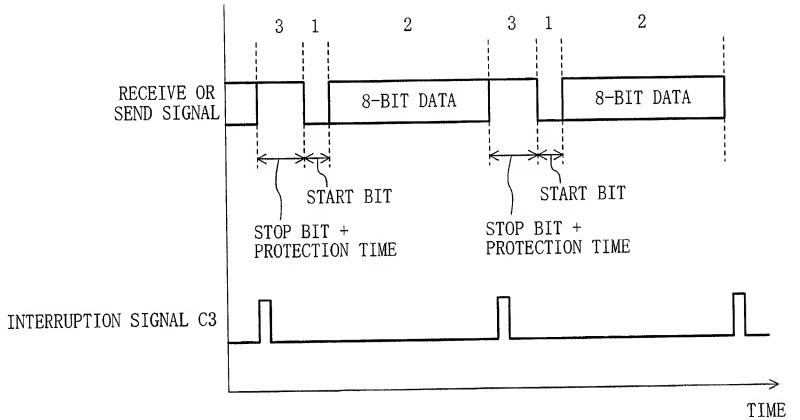
FIG. 5



10/030252

20607D*2520E0DT

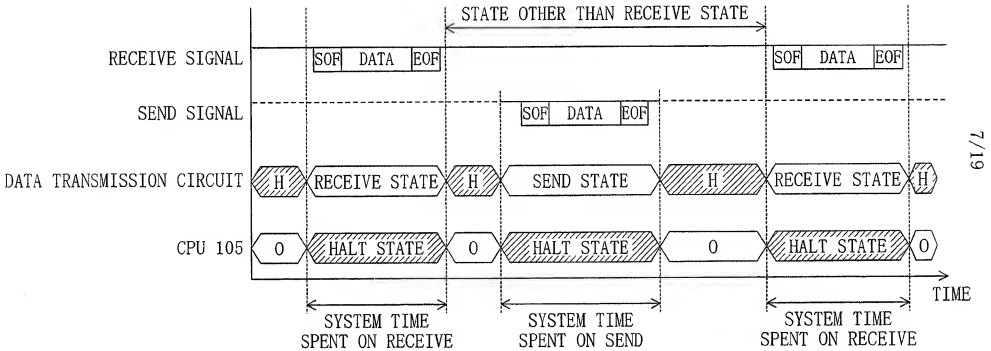
FIG. 6



10/030225

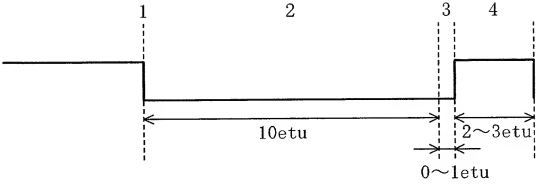
2060TD*2520E00T

FIG. 7



10/03252

FIG. 8



JP02/02520 06.10.2002

FIG. 9

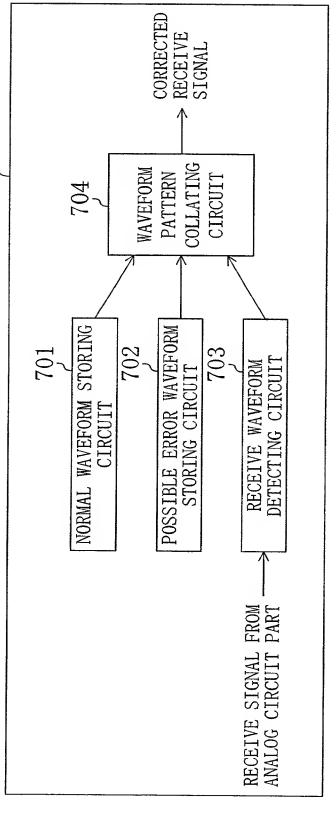
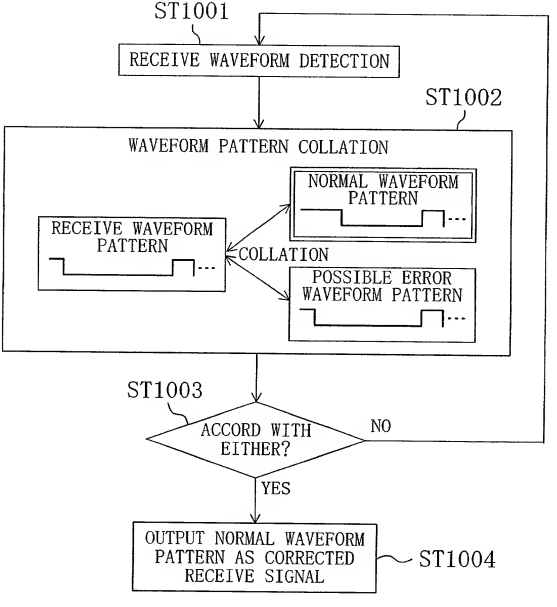

700
701
NORMAL WAVEFORM STORING CIRCUIT
702
POSSIBLE ERROR WAVEFORM STORING CIRCUIT
703
RECEIVE WAVEFORM DETECTING CIRCUIT
704
WAVEFORM PATTERN COLLATING CIRCUIT
CORRECTED RECEIVE SIGNAL
RECEIVE SIGNAL FROM ANALOG CIRCUIT PART

FIG. 10



2000TC*2520E001

FIG. 11

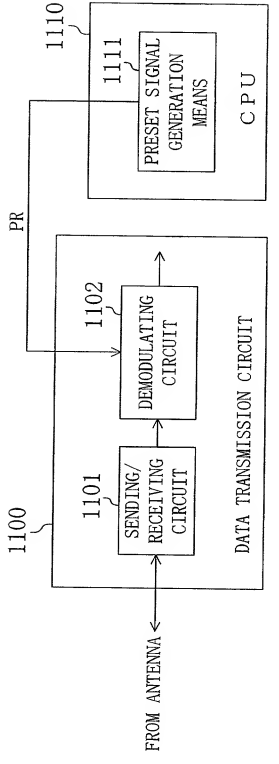
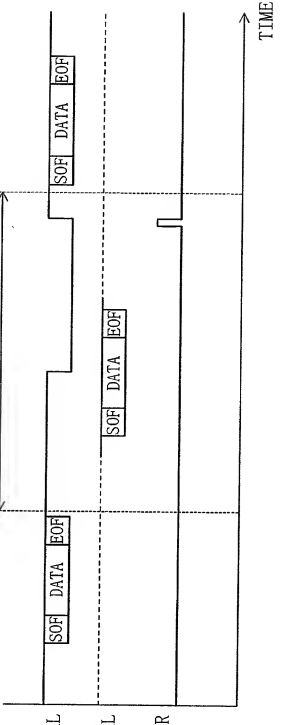
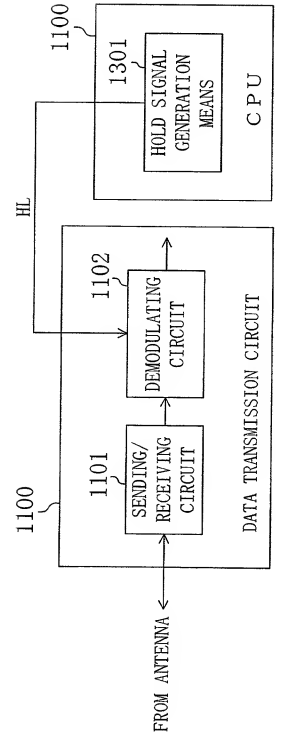

1110
1111
PRESET SIGNAL GENERATION MEANS
CPU
PR
1102
DEMODULATING CIRCUIT
1100
1101
SENDING/ RECEIVING CIRCUIT
DATA TRANSMISSION CIRCUIT
FROM ANTENNA

FIG. 12


RECEIVE SIGNAL
SEND SIGNAL
PRESET SIGNAL PR
SOF
DATA
EOF
SOF
DATA
EOF
SOF
DATA
EOF
STATE OTHER THAN RECEIVE STATE
TIME

2060TO'2520E00T

FIG. 13



20610"25208001

FIG. 14

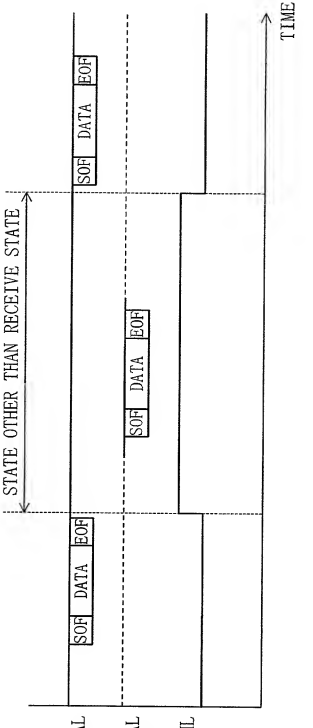
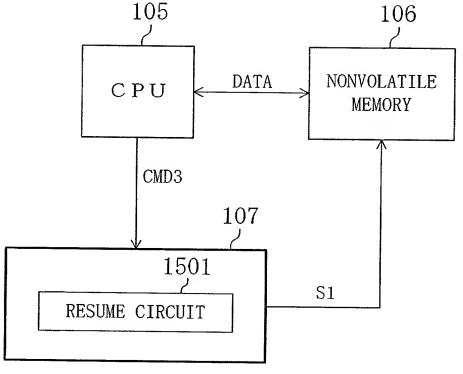
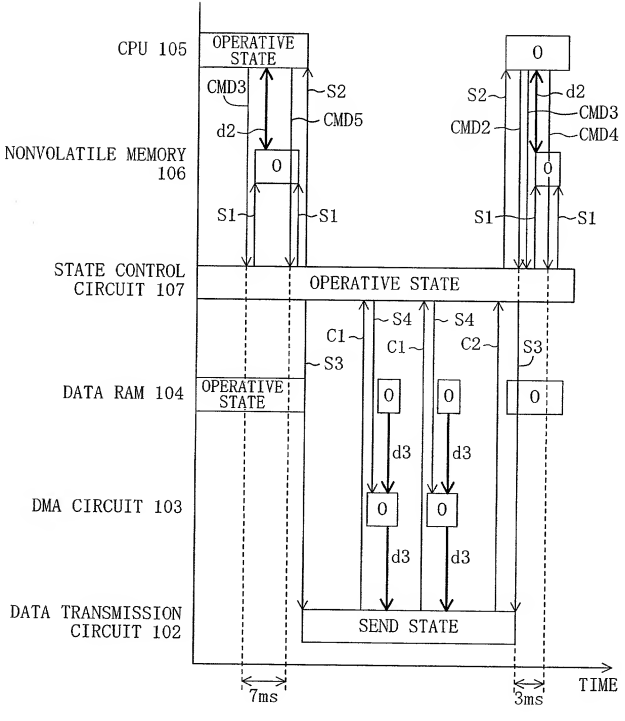


FIG. 15



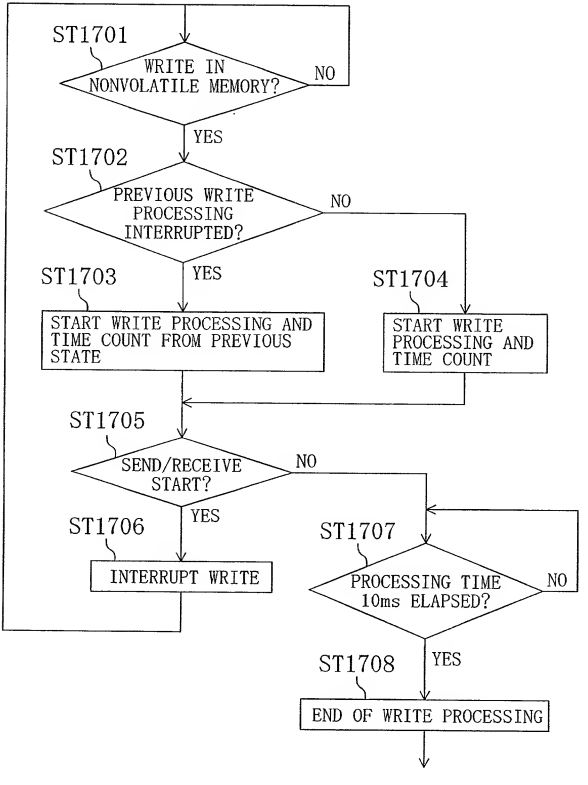
20040702.2520E01

FIG. 16



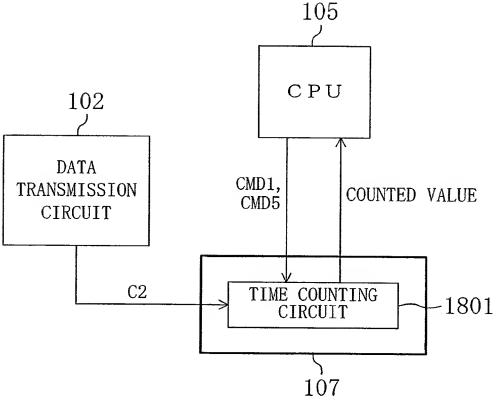
20040702.2520E001

FIG. 17



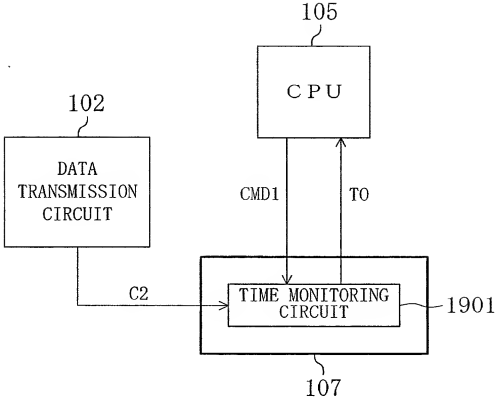
2060TO 25208001

FIG. 18



JP030252 2004.10.28

FIG. 19



JP03/25201 20010410